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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,403	07/07/2003	Eitan Rosen	MP0278	5933

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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 400
TROY, MI 48098

EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,403	ROSEN, EITAN	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *02/22/06*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered March 09, 2006.

- Claims 1-90 are pending. Claims 1, 13, 25, 36, 47, 58, 69, & 80 are amended.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1, 13, 25, 36, 47, 58, 69, & 80 and previously presented claims 2-12, 14-24, 26-35; 37-46, 48-57, 59-68, 70-79, & 81-90 filed March 09, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "that Sunter fails to disclose the limitation of changing a duration of m selected pulses." Further applicant contends that the invention is changing the frequency and not the selected pulses. The Examiner respectfully disagrees.

Sunter clearly states "At least one of the oscillator units has a plurality of programmable ring oscillators, each ring oscillator having multiple delay stages connected in series to form a ring, at least one of the delay stages having programmable delay to produce an internal clock signal with programmable frequency; and an oscillator **selector for selecting** the internal clock signal of one of said ring oscillators of the first oscillator unit. The circuit further

comprises a unit selector for **selecting one of the first and second oscillator** units as a main oscillator unit to produce the main clock signal form the internal clock signal of the main oscillator unit, and selecting the other one of the first and second oscillator units as a secondary oscillator unit to produce a secondary clock signal from the internal clock signal of the secondary oscillator unit......a frequency controller for adjusting the programmable frequency of the internal clock signal of the secondary oscillator unit and controlling the first and second oscillator selectors **to select a different ring oscillator** from the secondary oscillator unit, based on the comparison result; and a unit controller for controlling the unit **selector to switch the selection** between the main oscillator unit and the secondary oscillator unit when frequency adjustment of the secondary oscillator unit is completed" (columns 4-5, lines 51-13). It can clearly, be seen that Sunter is not changing the frequency of all the ring oscillators in fact the selector unit selects the ring oscillator, and then changes the duration of the frequency. There is definitely a selection process in place. Lastly, the length of the pulse is dependent on the frequency, and hence when you change frequency you are also changing the lengths of the pulses.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 12-20, 24-31, 35-42, 46-53, 57-64, 68-75, 79-86, & 90 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Sunter et al. US Pat no. 6,204,694 B1.

As per claim 1:

Sunter et al. teaches an apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus and method comprising, a control circuit adapted to provide a control signal (Figure 6B # 605, column 8, lines 45-51), and a signal generator adapted (column 4, lines 31-35) to, receive a first clock signal comprising k pulses each having a first duration, change the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k (column 5, lines 1-13) and the second duration is not substantially equal to the first duration, to produce a second clock signal, and apply the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60).

As per claim 2:

Sunter et al. teaches an apparatus further comprising a clock circuit adapted to provide the clock signal (column 4, lines 51-54).

As per claim 3:

Sunter et al. teaches an apparatus further comprising a measurement circuit adapted to measure a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7).

As per claim 4:

Sunter et al. teaches an apparatus further comprising a comparison circuit adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4).

As per claim 5:

Sunter et al. teaches an apparatus further comprising an analysis circuit adapted to identify one of the signal paths as flawed based on the test result (column 6, lines 59-65).

As per claim 6:

Sunter et al. teaches an apparatus where in the signal generator is further adapted to change the duration of every nth pulse of the signal to the second duration to produce the second clock signal (Fig 12B # 1250, columns 6-7, lines 66-5), and successively apply the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25).

As per claim 7:

Sunter et al. teaches an apparatus wherein n = 2 (column 4, lines 51-54).

As per claim 8:

Sunter et al. teaches an apparatus wherein the comparison circuit is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time

corresponding to one of the n different predetermined phases (column 7, lines 7-15), and wherein the analysis circuit identifies at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65).

As per claim 12:

Sunter et al. teaches an apparatus wherein the one of the clocked storage elements is part of a scan chain (column 7, lines 5-8); and wherein the measurement circuit is further adapted to shift the contents of the scan chain from the integrated circuit to the measurement circuit (column 7, lines 15-30).

As per claim 13:

Sunter et al. teaches an apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus comprising: control means for providing a control signal (Figure 6B # 605, column 8, lines 45-51); and signal generator means (column 4, lines 31-35) for receiving a first clock signal comprising k pulses each having a first duration, changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and the second duration is not substantially equal to the first duration, to produce a second clock signal, and applying the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60).

As per claim 14:

Sunter et al. teaches an apparatus clock means for providing the clock signal (column 4, lines 51-54).

As per claim 15:

Sunter et al. teaches an apparatus further comprising measurement means for measuring a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7).

As per claim 16:

Sunter et al. teaches an apparatus further comprising comparison means for comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4).

As per claim 17:

Sunter et al. teaches an apparatus further comprising analysis means for identifying one of the signal paths as flawed based on the test result (column 6, lines 59-65).

As per claim 18:

Sunter et al. teaches an apparatus wherein the signal generator means comprises: means for changing the duration of every nth pulse of the signal to the second duration to produce the second clock signal (Fig 12B # 1250, columns 6-7, lines 66-5); and means for successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25).

As per claim 19:

Sunter et al. teaches an apparatus wherein n = 2 (column 4, lines 51-54).

As per claim 20:

Sunter et al. teaches an apparatus wherein the comparison means comprises means for comparing the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15); and wherein the analysis means comprises means for identifying at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65).

As per claim 24:

Sunter et al. teaches an apparatus wherein the one of the clocked storage elements is part of a scan chain (column 7, lines 5-8); and wherein the measurement means further comprises means for shifting the contents of the scan chain from the integrated circuit to the measurement circuit (column 7, lines 15-30).

As per claims 25 and 36:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the method comprising: receiving a first clock signal comprising k pulses each having a first duration (Figure 6B # 605, column 8, lines 45-51); changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k and the second

duration is not substantially equal to the first duration (column 7, lines 11-15), to produce a second clock signal; and applying the second clock signal to clock inputs of a plurality of clocked storage elements interconnected by a plurality of signal paths in a circuit (column 4, lines 51-60).

As per claims 26 and 37:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method further comprising measuring a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7).

As per claims 27 and 38:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method further comprising comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4).

As per claims 28 and 39:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method further comprising identifying one of the signal paths as flawed based on the test result (column 6, lines 59-65).

As per claims 29 and 40:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method wherein changing the duration of m of the pulses comprises changing the duration of every nth pulse of

the signal to the second duration to produce the second clock signal (Fig 12B # 1250, columns 6-7, lines 66-5); and wherein applying the second clock signal to the clock inputs of the clocked storage elements comprises successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25).

As per claim 30 and 41:

Sunter et al. a method wherein n = 2 (column 4, lines 51-54) and n = 1 (column 6, lines 49-51).

As per claims 31 and 42:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method wherein comparing the signal generated by the integrated circuit to the predicted signal comprises comparing the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15); and wherein identifying one of the signal paths as flawed comprises identifying at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65).

As per claims 35 and 46:

Sunter et al. teaches a method and a computer program embodying instructions executable by a computer to perform a method wherein the one of the clocked storage elements is part of a scan chain (column 7, lines 5-8) further

comprising: shifting the contents of the scan chain from the integrated circuit to the measurement circuit (column 7, lines 15-30).

As per claims 47, 58, 69, and 80:

Sunter et al. teaches an apparatus, method and a computer program embodying instructions executable to perform a method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus comprising a control circuit and means adapted to provide a control signal (Figure 6B # 605, column 8, lines 45-51); and a signal generator and means adapted (column 4, lines 31-35) to produce a clock signal comprising j pulses each having the first duration and m pulses having a second duration in response to the control signal, wherein $k = m + j$ (As per claim 1 it was noted that $m < k$, hence the equation $k = m + j$ holds the same limitations and is rejected under column 5, lines 1-13), and wherein the second duration is not substantially equal to the first duration, to produce a clock signal, and apply the clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60).

As per claims 48, 59, 70, and 81:

Sunter et al. teaches an apparatus, method, and computer program further comprising a measurement circuit and measurement means adapted to measure a signal generated by the integrated circuit in response to the clock signal (column 5, lines 4-7).

As per claims 49, 60, 71, and 82:

Sunter et al. teaches an apparatus, method, and computer program further comprising a comparison circuit and means adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4).

As per claims 50, 61, 72, and 83:

Sunter et al. teaches an apparatus, method, and computer program further comprising an analysis circuit and analysis means adapted to identify one of the signal paths as flawed based on the test result (column 6, lines 59-65).

As per claims 51, 62, 73, and 84:

Sunter et al. teaches an apparatus, method, and computer program wherein m = nj (same as number of pulses as in claim 6) and every pulse of the clock signal having the first duration is followed by n pulses having the second duration (Fig 12B # 1250, columns 6-7, lines 66-5), wherein the signal generator and means is further adapted to successively apply the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25).

As per claims 52, 63, 74, and 85:

Sunter et al. teaches an apparatus, method, and computer program wherein n = 2 (column 4, lines 51-54).

As per claims 53, 64, 75, and 86:

Sunter et al. teaches an apparatus, method, and computer program wherein the comparison circuit and means is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15), and wherein the analysis circuit and means identifies at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65).

As per claims 57, 68, 79, and 90:

Sunter et al. teaches an apparatus, method, and computer program wherein the one of the clocked storage elements is part of a scan chain (column 7, lines 5-8); and wherein the measurement circuit and means is further adapted to shift the contents of the scan chain from the integrated circuit to the measurement circuit (column 7, lines 15-30).

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 9-11, 21-23, 32-34, 43-45, 54-56, 65-67, 76-78, & 87-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sunter et al. US Pat no. 6,204,694 B1, and further in view of Palermo US Pat no. 5,761,097.

As per claims 9, 10, and 11:

Sunter et al. substantially teaches an apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus comprising, a control circuit adapted to provide a control signal (Figure 6B # 605, column 8, lines 45-51), and a signal generator adapted (column 4, lines 31-35) to, receive a first clock signal comprising k pulses each having a first duration, change the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k and the second duration is not substantially equal to the first duration, to produce a second clock signal, apply the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60), further comprising a clock circuit adapted to provide the clock signal (column 4, lines 51-54), apparatus further comprising a measurement circuit adapted to measure a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7), further comprising a comparison circuit adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4), further comprising an analysis circuit adapted to identify one of the signal paths as flawed based on the test result (column 6, lines 59-65), where in the signal generator is further adapted to change the duration of

every nth pulse of the signal to the second duration to produce the second clock signal (Fig 12B # 1250, columns 6-7, lines 66-5), and successively apply the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25), wherein n = 2 (column 4, lines 51-54), wherein the comparison circuit is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15), and wherein the analysis circuit identifies at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65), wherein the comparison circuit is further adapted to compare values stored in the clocked storage elements to predicted values (column 7, lines 9-14), wherein the comparison circuit is further adapted to compare a value stored by one of the clocked storage elements to a corresponding one of the predicted values (column 7, lines 9-14), and wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values (column 6, lines 56-65), wherein the comparison circuit is further adapted to compare the value stored by a further one of the clocked storage elements to a further- corresponding one of the predicted values (column 7, lines 5-15), wherein the value stored by the one of the clocked storage

elements is a function of the value stored by the further one of the clocked storage elements (column 7, lines 11-25) and wherein the analysis circuit is further adapted to identify is flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values (column 7, lines 17-25 & column 6, lines 59-65).

Sunter et al. does not explicitly teach the signal generator to be further adapted to apply the failure phase of the clock signal.

However, Palermo, in an analogous art, teaches an apparatus wherein the signal generator is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time (Figure 5 # 112, column 6, lines 43-55) and wherein the signal generator is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values (Figure 5 # 110, column 6, lines 25-55). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the failure phase to the clock inputs within the signal generator of Sunter at al. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that applying the failure phase would have ensured a better analysis of the timing violations.

As per claim 21-23, 32-34, and 43-45:

Sunter et al. substantially teaches an apparatus, a method, and a computer program embodying instructions executable by a computer to perform a method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus comprising: control means for providing a control signal (Figure 6B # 605, column 8, lines 45-51); and signal generator means (column 4, lines 31-35) for receiving and producing a first clock signal comprising k pulses each having a first duration, changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k and the second duration is not substantially equal to the first duration, to produce a second clock signal, and applying the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60), an apparatus clock means for providing the clock signal (column 4, lines 51-54), further comprising measurement means for measuring a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7), further comprising comparison means for comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4), further comprising analysis means for identifying one of the signal paths as flawed based on the test result (column 6, lines 59-65), wherein the signal generator means comprises: means for changing the duration of every nth pulse of the signal to the second duration to produce the second clock signal (Fig 12B # 1250, columns 6-7, lines

66-5); and means for successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25), wherein n = 2 (column 4, lines 51-54), wherein the comparison means comprises means for comparing the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15); and wherein the analysis means comprises means for identifying at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65), wherein the comparison means further comprises means for comparing values stored in the clocked storage elements to predicted values, (column 7, lines 9-14) wherein the comparison means further comprises means for comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values (column 7, lines 9-14), wherein the analysis means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values result (column 6, lines 59-65), wherein the comparison means further comprises means for comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values (column 6, lines 56-65), wherein the value stored by the one of the clocked storage elements is a function of the value stored by the

further one of the clocked storage elements (column 7, lines 5-15), and wherein the analysis circuit means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values (column 7, lines 17-25 & column 6, lines 59-65).

Sunter et al. does not explicitly teach the signal generator to be further adapted to apply the failure phase of the clock signal.

However, Palermo, in an analogous art, teaches an apparatus, a method, and a computer program embodying instructions executable by a computer to perform a method wherein the signal generator means further comprises means for applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time (Figure 5 # 112, column 6, lines 43-55) and wherein the signal generator means further comprises means for applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values (Figure 5 # 110, column 6, lines 25-55). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the failure phase to the clock inputs within the signal generator of Sunter at al. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the

art would have recognized that applying the failure phase would have ensured a better analysis of the timing violations.

As per claims 54-56, 65-67, 76-78, and 87-89:

Sunter et al. substantially teaches an apparatus, method, and computer program for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (column 4, lines 21-26), the apparatus, method, and computer program comprising, a control circuit and means adapted to provide a control signal (Figure 6B # 605, column 8, lines 45-51), and a signal generator and means adapted (column 4, lines 31-35) to, producing a first clock signal comprising k pulses each having a first duration, change the duration of each of m of the pulses to a second duration in response to the control signal, wherein k = m + j and the second duration is not substantially equal to the first duration, to produce a second clock signal, apply the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60), further comprising a clock circuit adapted to provide the clock signal (column 4, lines 51-54), apparatus, method, and computer program further comprising a measurement circuit and means adapted to measure a signal generated by the integrated circuit in response to the second clock signal (column 5, lines 4-7), further comprising a comparison circuit and means adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result (column 5, lines 1-4), further comprising an analysis circuit and means adapted to identify one of the signal paths as flawed

based on the test result (column 6, lines 59-65), wherein m = nj (relates to number of pulses as in claim 6) and very pulse of the clock signal having the first duration is followed by n pulses having the second duration (Fig 12B # 1250, columns 6-7, lines 66-5), wherein the signal generator and means is further adapted to successively apply the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements (column 7, lines 17-20), wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal (column 7, lines 21-25), wherein n = 2 (column 4, lines 51-54), wherein the comparison circuit and means is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times (Fig 12A # 1252, column 7, lines 6-7), each time corresponding to one of the n different predetermined phases (column 7, lines 7-15), and wherein the analysis circuit and means identifies at least one of the n different predetermined phases as a failure phase (column 6, lines 59-65), wherein the comparison circuit and means is further adapted to compare values stored in the clocked storage elements to predicted values (column 7, lines 9-14), wherein the comparison circuit and means is further adapted to compare a value stored by one of the clocked storage elements to a corresponding one of the predicted values (column 7, lines 9-14), and wherein the analysis circuit and means is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values (column 6, lines 56-65), wherein the comparison circuit and

means is further adapted to compare the value stored by a further one of the clocked storage elements to a further- corresponding one of the predicted values (column 7, lines 5-15), wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements (column 7, lines 11-25) and wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values (column 7, lines 17-25 & column 6, lines 59-65).

Sunter et al. does not explicitly teach the signal generator to be further adapted to apply the failure phase of the clock signal.

However, Palermo, in an analogous art, teaches an apparatus, method, and computer program wherein the signal generator and means is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time (Figure 5 # 112, column 6, lines 43-55) and wherein the signal generator and means is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values (Figure 5 # 110, column 6, lines 25-55). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the failure phase to the clock inputs within the

signal generator of Sunter at al. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that applying the failure phase would have ensured a better analysis of the timing violations.

Claims 1, 13, 25, 36, 47, 58, 69, and 80, are also rejected under 35 U.S.C. 103(a) as being unpatentable over Liguori US Pat no. 6,059,836, and further in view of Sunter et al. US Pat no. 6,204,694 B1.

As per claims 1, 13, 25, 36, 47, 58, 69, and 80 Liguori substantially teaches an apparatus, method, means, and computer program for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input wherein the clocked storage elements are interconnected by a plurality of signal paths (Fig 1, #4, column 3, lines 48-50), the apparatus, method, means, computer program and method comprising, a control circuit adapted to provide a control signal (Fig 1, #6, column 3, lines 51-53).

Liguori does not substantially teach a signal generator adapted to, receive and produce a first clock signal comprising k pulses each having a first duration, change the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k and the second duration is not substantially equal to the first duration, to produce a second clock signal, and apply the second clock signal to the clock inputs of the plurality of clocked storage elements.

However, Sunter et al., in an analogous art, teaches an apparatus, method, means, and a computer program comprising a signal generator and

means adapted (column 4, lines 31-35) for receiving a first clock signal comprising k pulses each having a first duration, changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and $k = m + j$ (column 5, lines 1-13) and the second duration is not substantially equal to the first duration, to produce a second clock signal, and applying the second clock signal to the clock inputs of the plurality of clocked storage elements (column 4, lines 51-60). This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that applying multiple levels of testing would have ensured a better analysis of the circuit.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 4,893,072 A1, US Pat no. 6,266,749 B1, US Pat no. 5,053,698 A, US 5,099,196 A and US Pat no. 5,325,369 A mention the same apparatus for testing an integrated circuit are included herein for Applicant's review.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
04/10/2006

GUY LAMARRE
PRIMARY EXAMINER